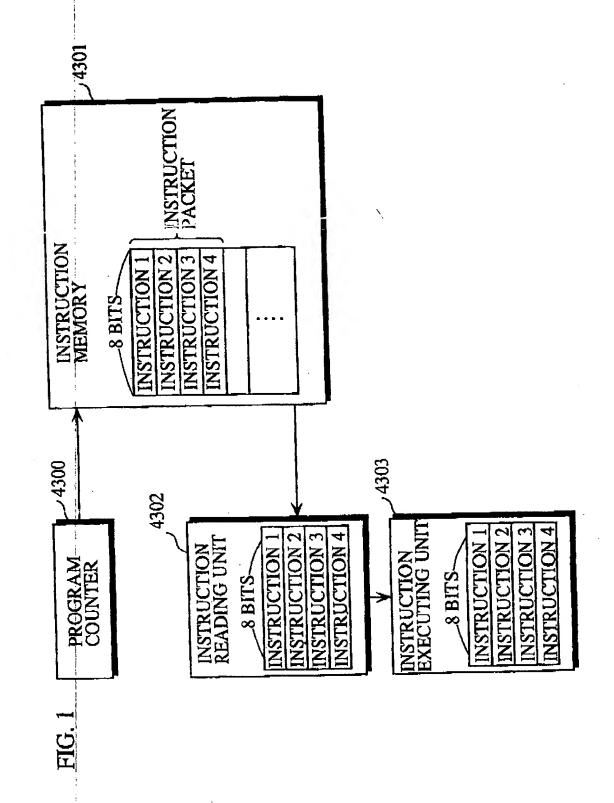
ソ



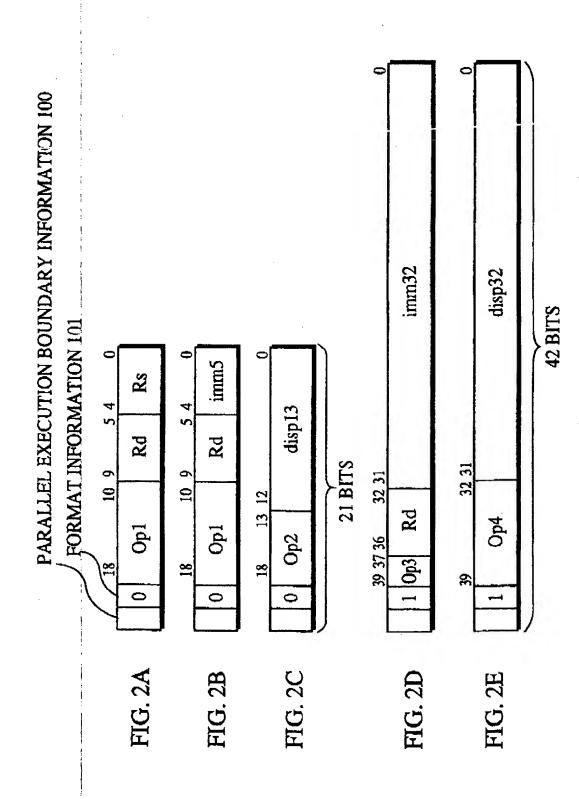
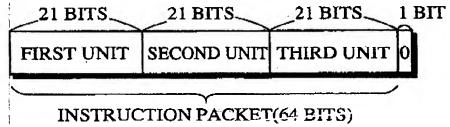
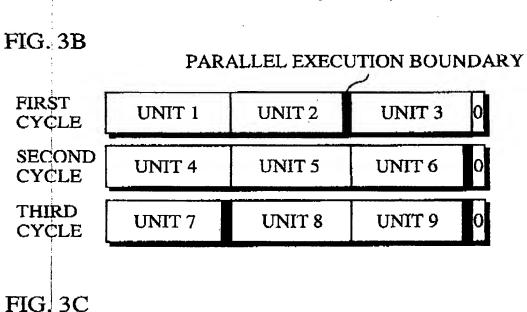


FIG. 3A





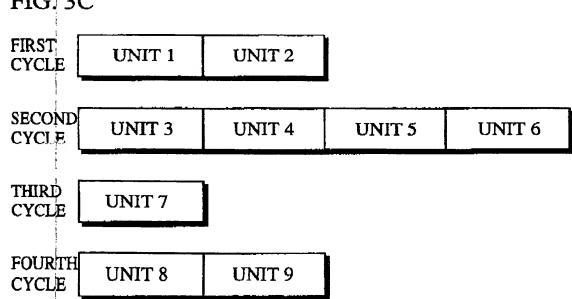


FIG. 4

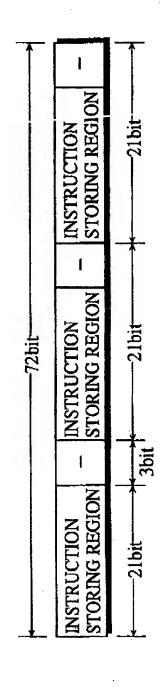


FIG. 5

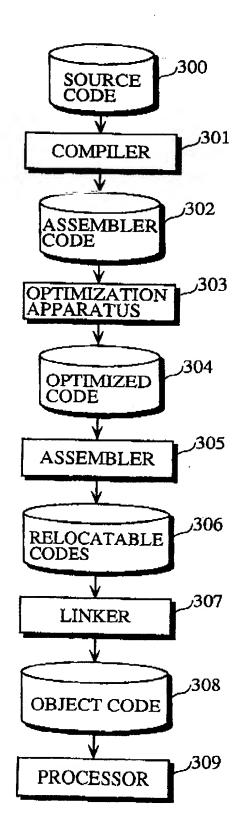


FIG. 6 402 FIRST CALCU-TIMDY ALCU-VATOR SECONDICALCIL REGISTERS 401c 401a 401b 32 405 **L**3 411 29 **\$**29 29 . 3 UPPER PC LOWER PC LOWER PC CALCULATOR PPER PC CALCULATOR INC [\]403 412 29 carry .29 32 32 3 421 29 420 PC RELATIVE VALUE SELECTOR IMMEDIATE SELECTOR OPERAND 423 DATA BUFFER CONTROL SIGNAL 1246 OPERAND ADDRESS BUFFER SECOND INSTRUCTION DECODER FIRST INSTRUCTION DECODER THIRD INSTRUCTION DECODER 410 PREFETCH UPPER COUNTER +1 409c 409ь 406 21 21 21 PREFETCH LOWER COUNTER DATA MEMORY FIRST SECOND THURD UNIT UNIT UNIT \3 29 ⁴¹³ INSTRUCTION MEMORY INSTRUCTION PACKET 64 407 408 INSTRUCTION BUFFER

-- FIG --

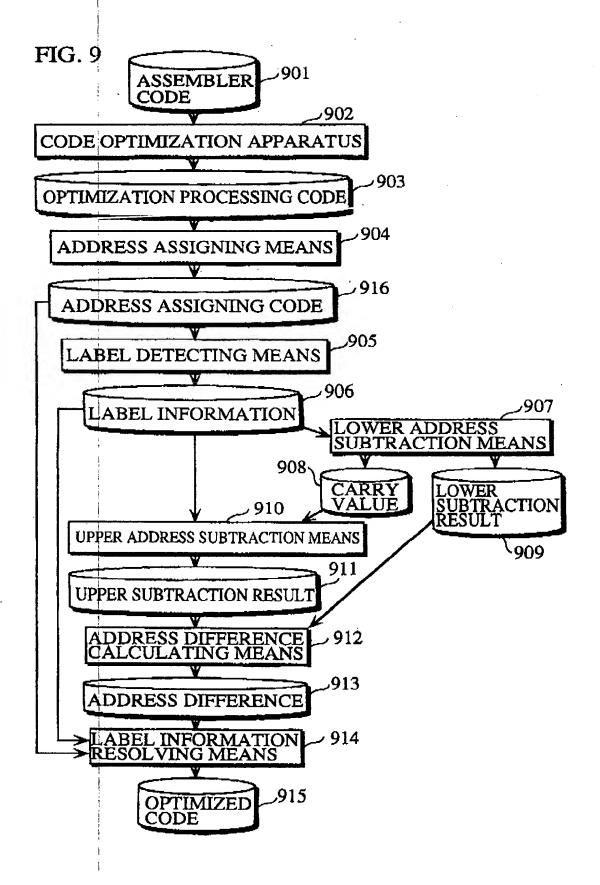
IN-PACKET ADDRESS BEFORE UPDATING VALUE	3,2000	3'b010	3'5100
1	3'5010	3'b100	3'b000 (CARRY 1)
2	3,9100	3'b000 (CARRY 1)	3'b010 (CARRY 1)
3	3'b000 (CARRY 1)	3'b010 (CARRY 1)	3'b100 (CARRY 1)
4	3'b010 (CARRY 1)	3'b100 (CARRY 1)	3'b000 (CARRY 2)

FIG. 8A

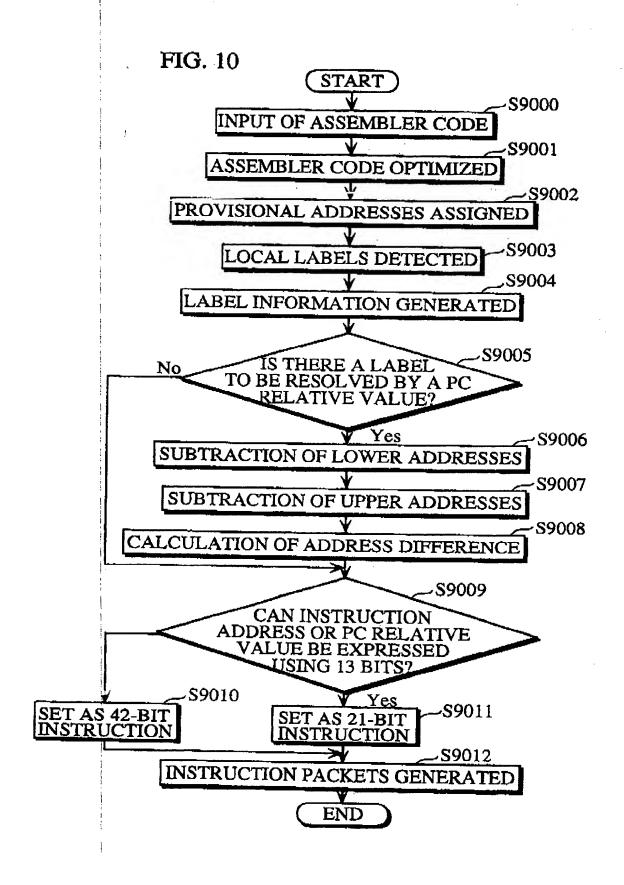
LOWER 3 BITS OF ADDRESS LOWER 3 VALUE BITS OF PC RELATIVE VALUE	;	3"b010	3'b100
3'b000	3'6000	3'b010	3'b100
3'b010	3'b010	3'b100	3'b000 (CARRY 1)
3'b100	3'ь100	3'b000 (CARRY 1)	3'b010 (CARRY 1)

FIG. 8B

LOWER	LOWER 3 BITS OF ADDRESS VALUE(TO BE SUBTRACTED)			
OF ADD	RESS	_		
SUBTR	(BEFORE ACTION)	3'b00	06010	Ob100
			<u> </u>	
	3'ь000	3'6000	3'b100	3'ь010
			(CARRY 1)	(CARRY 1)
:	3'b010	3'ъ010	3'b000	3'6100
	211.100			(CARRY 1)
	3'b100	3'Ь100	3'b010	3'Ъ000
	•			



Ξ



FIG, 11

L1:	mov r2, r1		•	1000
	jsr f			1001
	add r0, r4		•	· 1002
	and r1, r3		1	• 1003
	mov L2, r2			1004
	ld (r2), r0			1005
	bra L1	1		1006
	add r2, r3	•		1007
•••				
L2:	•••	•	•	1008

FIG. 12

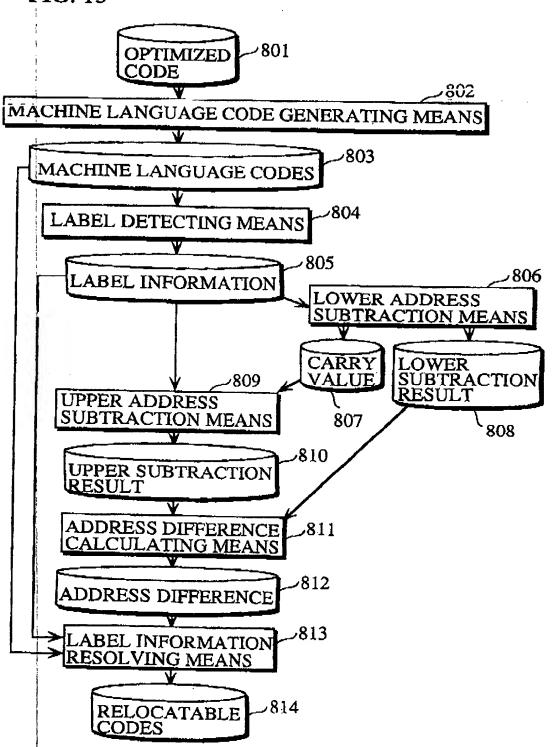
32'h00000800	L1: mov r2, r1	• 1000
32'h00000802	jsr f	· · 1001
32'h00000804	add r0, r4	• 1002
32'h00000808	and r1, r3	· · 1003
32'h0000080a	mov L2, τ2	· · 1004
32'h00000810	ld (r2), r0	• • 1005
32'h00000812	bra L1	· · 1006
32'h00000814	add r2, r3	• • 1007
	•••	1007
32'h12345678	L2:	• 1008

INSTRUCTION	RESOLVING VALUE	
mov L2, r2	ADDRESS	32'h12345678
bra L1	PC RELATIVE VALUE	32h00000800-32h00000812

```
L1: mov r2, r1 || jsr f || add r0, r4 | · · 1300 |
and r1, r3 || mov L2, r2 || (mov L2, r2) | · · 1301 |
ld (r2), r0 || bra L1 || add r2, r3 | · · 1302 |
...

L2: · · 1303
```

FIG. 15



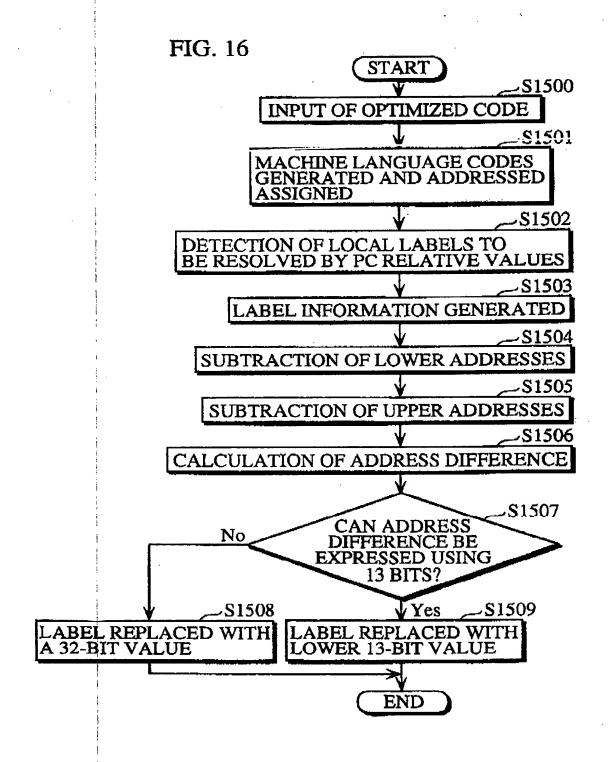


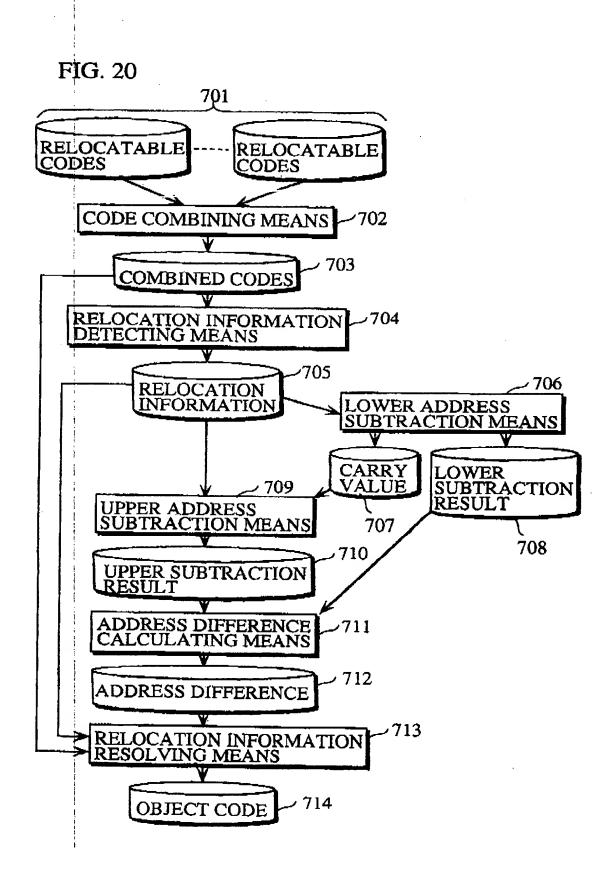
FIG. 17

	0.1400		•	1411	7 7 7
	add r0, r4 ··· 1403	1	add r2, r3 ···1410		
	jsr f1402	mov L2, r2 ···1406	ld (r2), r0 ···1408 bra L1 ···1409		
1	l: mov r2, r1 ··· 1401 jsr f	and r1, r3 ···1405	ld (r2), r0 ···1408	2:	
	29/h00000000 L1:	29'h000000001	29'h00000002	29'h02468acf L2	

INSTRUCTION	RESOLVING VALUE	
bra L1	PC RELATIVE VALUE	32'h00000000-32'h00000012

FIG. 19

UNUSED BIT AREA	• 1600	· 1604	. 1607		0 • • • 1611
UNIT ARE	<u>Ö</u>	0	<u>.</u>		0
	1603		1610		
	r4.		r3 ::		
	1602 0:0; add r0, r41603 0		dd r2,		
	0. ac		0; a		
	2 0	9091	060		
o takan to taka	160	•	16		
	•	2, r2	h1fec		
, X	sr f	nd r1, r3 1605 11 1 mov L2, r2 1606	l (r2), r0 ···1608 1;0;bra 13'h1fec···1609 0;0; add r2, r3 ···1610 0		
MAT	1.0.1	4 111	1.0.1		
BIT FORMAT INFORMATION	1601	1605	1608		:
BIT INF(:	3	0		
z\	v 12,	rl, r	(2)		
ON ATIO	no	and]d (
SEM /	1.L1:			:	L2:
XEC INF	0:0	0.0	0.0		
PARALLEL EXECUTION BOUNDARY INFORMATION	29'h00000000 0'0'L1: mov r2, r1 ···1601 1'0'jsr f	29'h00000001 0:0	29'h00000002 0:0		29'h02468acf
ALL ND	0000	9000	0000		0246
PAR BOL	29'h	29'h	29'h		29'h



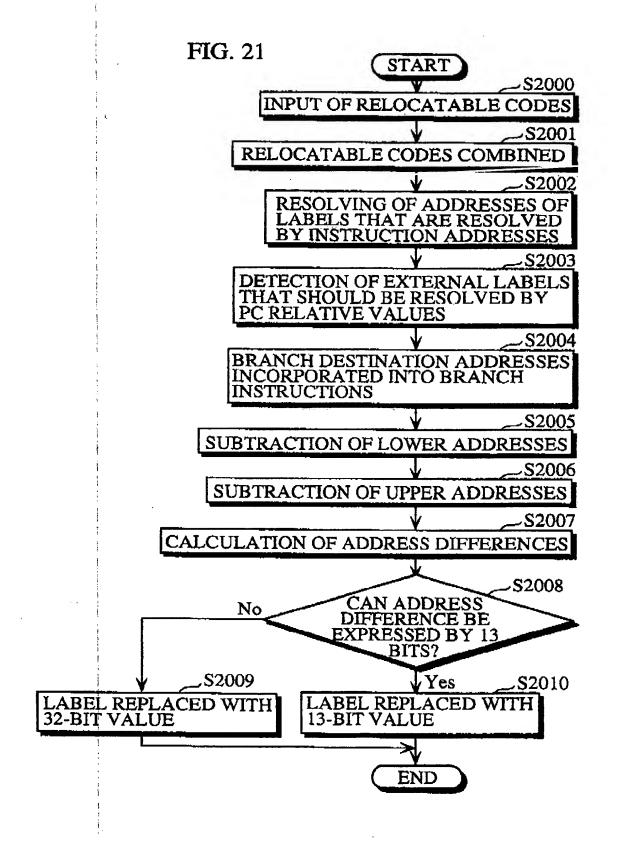


FIG. 22

1707	
•	
lou	
1702 [1:0]	
dou	
1701 0:0	
ret	
29'h00000000 0:0;f:	

1803 0 1800	18070 1804	0 · · 1808	18140 1811		0 · · 1815
	1806 0:0; add r0, r41807 0		add r2, r3		
1.0	0.0	10	0.0		
···1802 1:0 nop	1806	L2, r2 ···18	3h1fec…1813		
0 0 nop	1 0 jsr f	1 1 mov	1 0 bra 1		
ret1801 0;0;nop	mov r2, r1 ···1805 1; 0; jsr f	and r1, r3 ···1809 1; 1; mov L2, r2 ···1810	ld (r2), r01812 [1]0;bra 13h1fec1813 [0;0] add r2, r31814 [0		••
	٠	0.0		•	L2:
29'h000000000 0:0 f.	29'h000000001 0 0 L1	29'h000000002 0¦0	29'h00000003 0¦0		29'h02468ad0

FIG. 24

,	. 1900	7001	1904	1000	1908	1011	1171		. 1015	C121
İ	. 1903 U	1906 10:0: add no nd 1907 of	170/10	21910	0	10 add 10 13 1014 0	10 121 121 121		U	2
ret1901 0:01non1907) 9061 1.181.11.11.11.71.47.1.1.1.1.1.1.1.1.1.1.1.1	and r1 r2 1000 1111	mm 11, 12 1709/11,1,mov 52,h12345680, 12	(4) 17	10 (12), 101912/1:0/bra 13/h1fec1913/0:0; add r2 r31014/n		• • •		
29'h000000000 [6:0 :f:	29'h000000001 0:0 1 1.	100	29/h000000002 0:0:	- C- C	29'h00000003 0:0			29'h02468ad0 L2:		

INSTRUCTION	RESOLVING VALUE
jsr f	PC RELATIVE VALUE 32'h00000000-32'h0000000a
	32 10000000a

· 2100	. 2104	. 2108	2111		0 · · 2115
•	. •				•
2103 0	r4 ···2107 0	0	r3 ···21140		0
dou	add r0,	2110	add r2,		
1:0;	0,0	12	0:0		
2101 0:0:nop2102 11:0: nop	mov r2, r1 ···2105 1;0; jsr 13'h1ff4···2106 0;0; add r0, r4 ···2107 0	and r1, r32109 1; 1; mov 32h12345680, r2	1d (r2), r02112 1:0 bra 13 h1fec 2113 0:0; add r2, r3 2114 0		•••
ret	mov r2	and r1,	ld (r2)		
0.0 f:	0 0 L1:	00	0.0	:	1.2:
29'h000000000 0:0 f:	29'h000000001 0 0 L1	29'h000000002 0 0 0	29'h000000003 0'0		29'h02468ad0

						A STATE OF THE PARTY OF THE PAR	The second second				
29'h00000000 0:0 f.	0 f.	ret	···2201 0:0 nop	0.0 nop	···2202 1:0 nop	1.0		2203 0	0	-	. 2200
29'h00000001 0;0 L1:	0¦L1:	mov r2, r1	2205	mov r2, r12205 1 0 jsr 13 h 1 ft8 2206 0 0 0; add r0, r4 2207 0	f8···2206	0.0	add r0, r4	2207	0		. 2204
29'h000000002 0;0	0	and rl, r3	2209	and r1, r32209 11,11,mov 32,h12345680, r2	12345680,	2	2210		0		. 2208
29'h00000003 0:0	0	ld (r2), r0	2212	ld (r2), r02212 1:0:bra 13'h1ff02213 0:0: add r2, r32214 0	ff02213	100	add r2, r3	2214		. 2	. 2211
	:								_		
29'h02468ad0	L2:		:						Ō	. 2215	215

FIG. 28A

	8 BITS	BIGHTH	
		SIXTH SEVENTH EIGHTH UNIT	-BIT)
	8 BITS 8 BITS 8 B	SIXTH	INSTRUCTION PACKET(64-BIT)
	8 BITS	FIFTH	CTION PA
	8 BITS	THIRD FOURTH FIFTH UNIT	INSTRU
	8 BITS	THIRD	
!	8 BIIS 8 B	SECOND	
Surface of	S BILLS	FIRST	
	i.		

FIG. 28C

מפני בוני	110.200	
710, 28B	IN-PACKET ADDRESS	UNIT
2-UNIT	3,5000	FIRST UNIT
INSTRUCTION	3'b001	SECOND UNIT
	3'b010	THIRD UNIT
3-UNIT INSTRUCTION	3'b011	FOURTH UNIT
	3.0100	FIFTH UNIT
5-UNIT INSTRUCTION	3'b101	SIXTH UNIT
	375110	SEVENTH UNIT
5-UNIT INSTRUCTION	3'b111	EIGHTH UNIT

FIG. 29A

LOWER BITS OF	PC	<u>ვ</u> ზ000	3'b010	3'b100
RELATI	VE VALUE	5 0000	3 0010	J 0100
	3'b000	3'b000	3'b010	3'b100
	3'b010	3'b010	3'b100	3'b000 (CARRY IGNORED)
	3'b100	3'b100	3'b000 (CARRY IGNORED)	3'b010 (CARRY IGNORED)
FIG.	29B			
	LOWER 3 BITS OF ADDRESS VALUE (TO BE SUBTRACTED)			
LOWER 3 OF ADDR VALUE (I BE SUBT	ESS	3'5000	3'b010	3'b100
	3'b000	3'6000	3'b100 (CARRY IGNORED)	3'b010 (CARRY IGNORED)
	3'b010	3'b010	3'b000	3'b100 (CARRY IGNORED)
	3'b100	3ъ100	3Ъ010	3'b000

2010 0000000000000000000000000000000000	" " " " " " " " " " " " " " " " " " "	03/0	•	004C 101E0AC
29 nonononon (2)	don join 2047 donio jo 1047 191	3		2
29'h000000001 0;0;L1:	1: mov r2, r1 ··· 2405 1 0 jsr 13 h1ffc ··· 2406 0 0 0; add r0, r4 ··· 2407 0 · · 2404	07/0	• .	. 2404
29'h000000002 0'0'	and r1, r32409 1;1 mov 32 h12345680, r22410	0	• .	• 2408
29'h00000003 0!0	ld (r2), r02412 1:0;bra 13h1ff42413 0:0; add r2, r32414 0 2411	140	•	. 2411
•				
29'h02468ad0 L2:	•••	0	•	0 · · 2415

FIG. 31A

LOWER 3 BITS OF ADDRESS VALUE BITS OF PC RELATIVE VALUE		3'b010	3'b100
3'ь000	3'b000	3'b000	3'b000
3'b010	3'b010	3'b010	3'b010
3'b100	3'b100	3'b100	3'b100

FIG. 31B

7	OWER 3 BITS OF ADDRESS VALUE			
	ER 3 OF PC ATIVE VALUE	3'b000	0b010	0b100
	3'b000	3'b000	3'b000	3'b000
	3'b010	3'b010	25010	215.01.0
	30010	20010	3'b010	3'ь010
	3'b100	3'b100	3'b100	3'b100

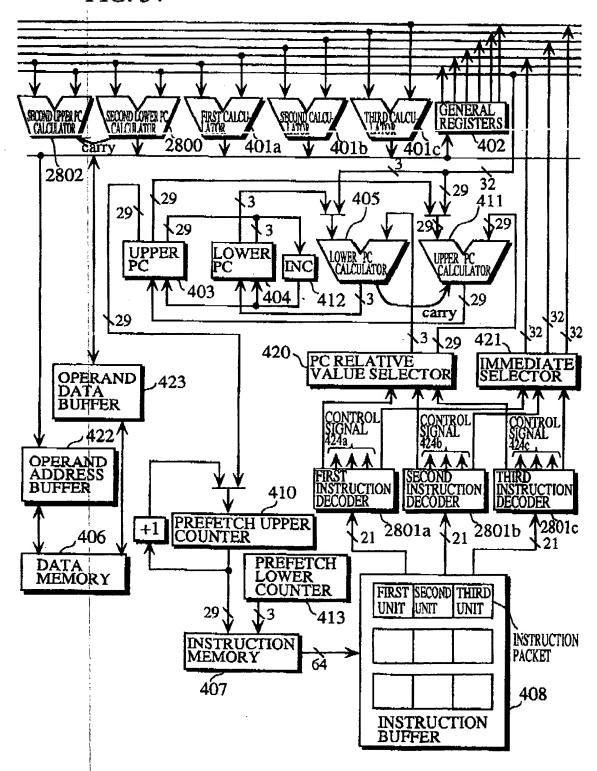
FIG. 3%

	١					2000			
29'h000000000 0;0;t:	Ţ.	ret2601 0:0 nop	0:0.0 lo	1:0: D				2600	
29'h00000001 0:0 L1	11	mov r2, r1 ··· 2605	mov r2, r1 ··· 2605 1:0; jsr 13 h1ff8 ··· 2606 0:0; add r0, r4 ··· 2607 0	0 0 ac	td r0, r4: ··	26070	-	2604	
29'h000000002 0 0		and r1, r3 ··· 2609	and r1, r3 ··· 2609 1; 1; mov 32'h12345680, r2 ··· 2610	21	.2610	0	•	. 2608	
29'h00000003 0,0		ld (r2), r0 ···2612	ld (r2), r0 …2612 1:0;bra 13;h1ff0 …2613 0;0; add r2, r3 …2614 0 · · · 2611	0;0; ac	ld r2, r3 ··	26140	:	. 2611	
29'h02468ad0	L2:	•••				0	•	0 · · 2615	

FIG. 33

. 2700	. 2704	. 2708	. 2711		. 2715
•	•	•	•		•
2703 0	127070	0	3 27140		0
1.0 nop	mov 12, 112705 1;0;jsr 13'h1ff62706 0;0; add 10, r42707 0	22710	ld (r2), r02712 1;0;bra 13;h1fee2713 0;0; add r2, r327140		
2702 11:0 nop	1ff62706 (and 11, 132709 1; 1;mov 32h12345680, 12	1fee ··· 2713 (
···2701 0 0 nop	1:0 jsr 13'h	1;1;mov 32	1:0 bra 13th		
2701	rl ···2705	r3 ···2709	r0 ···2712		:
ret	mov r2,	and r1,	ld (r2),		
0 0 f.	0 0 T	0 0	0:0	:	L2:
29'h00000000 0 0 f.	29'h000000001 0'0'L1	29'h00000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	29'h00000003 0:0		29'h02468ad0

FIG. 34



MNEMONIC

OPERATION

FIG. 35A ad

addpc disp, Rn

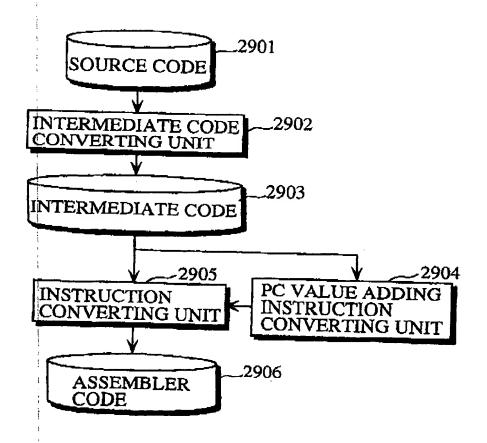
Rn + disp -> Rn

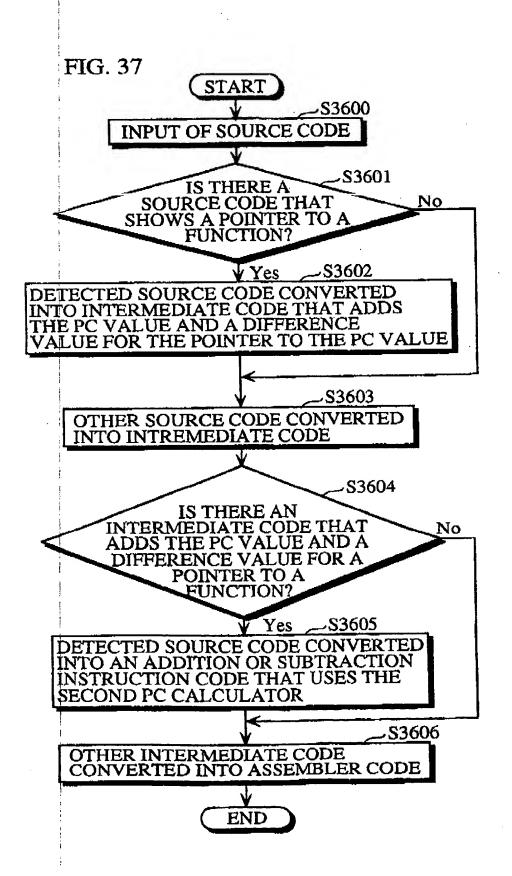
FIG. 35B

subpc disp, Rn

Rn-disp->Rn

FIG. 36





```
extern int g1();
extern int g2();
extern int g3();
extern int g4();

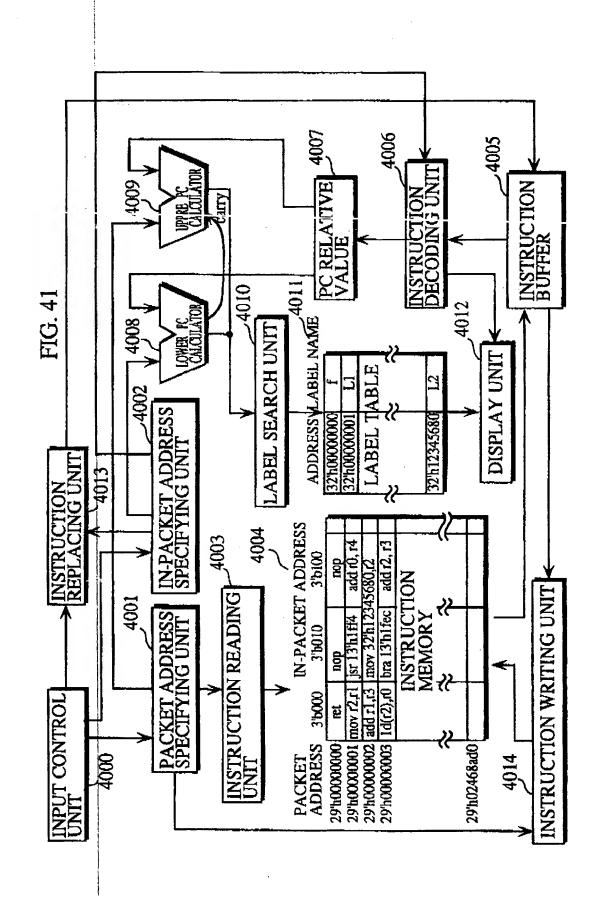
f(int i)
{
    int (*fp)();
    switch(i) {
        case 1: fp = g1;
            break;
        case 2: fp = g2;
            break;
        case 3: fp = g3;
            break;
        default: fp = g4;
}

(*fp)();
}
```

f:	tmp = PC	3201
	i ! = 1	3202
	br L1	3203
	fp = (g1 - f) + tmp	3204
	jmp L	3205
L1:	i ! = 2	3206
	br L2	3207
	fp = (g2 - f) + tmp	3208
	jmp L	3209
L2:	i ! = 3	3210
	br L3	3211
	fp = (g3 - f) + tmp	3212
	jmp L	3213
L3:	fp = (g4 - f) + tmp	3214
L:	* (fp) (i)	3215

f :	mov	PC, rl	3201
	compne	1, r0	3202
•	br	L1	3203
	addpc	g1-f, r1	3204
	jmp	L	3205
L1:	cmpne	2, r0	3206
	br	L2	3207
	addpc	g2-f, r1	3208
	jmp	L	3209
L2:	cmpne	3, r0	3210
	br	L3	3211
	addpc	g3-f, r1	3212
	jmp	Ĺ	3213
L3:	addpc	g4-f, r1	3214
L:	jsr ¯	(r1)	3215
	ret	- •	3216

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